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APPLICATION

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TITLE: ADAPTIVE CACHE ALGORITHM FOR TEMPERATURE SENSITIVE MEMORY

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ADAPTIVE CACHE ALGORITHM FOR TEMPERATURE SENSITIVE MEMORY

Background

This invention relates generally to electronic memories which may be sensitive to higher temperature environments.

In many cases, electronic memories may be subjected to higher temperature operating environments. For example, within a notebook or mobile personal computer, elevated temperatures may be encountered. Some types of memory may cease to function correctly at extended temperatures.

Ferroelectric polymer memory uses a polymer between a pair of electrodes. Ferroelectric polymer memories may be subject to voltage based disturbs at higher temperatures. At higher temperatures, a ferroelectric polymer memory may slow down its operation in order to function correctly.

This tendency to reduce speed at extended temperatures may complicate the operation of the system which relies on the ferroelectric polymer memory or other temperature sensitive memories. The slower data transfer rate may be unexpected by the rest of the system, since the remainder of the system may not be aware of the higher temperature conditions. Thus, the unexpected speed reduction may create unexpected problems in processor-based systems that rely on these memories, for example for caching purposes.

Thus, there is a need for a way to adapt processor-based systems to temperature sensitive memories.

Brief Description of the Drawings

Figure 1 is a schematic depiction of one embodiment of the present invention;

Figure 2 is a state diagram for a cache driver in accordance with one embodiment of the present invention; and

Figure 3 is a flow chart for one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a processor-based system 10 may be any conventional processor-based system, including mobile systems that operate on battery power. Examples of mobile systems include laptop computers, personal digital assistants, digital cameras, and cellular telephones. However, the present invention may be applicable to any of a wide range of processor-based systems.

The system 10 may include a processor 12 coupled in one architecture to a memory control hub 16. The hub 16 may in turn be coupled to an input/output control hub 18 in that architecture. The input/output control hub 18 may be coupled to a disk drive 20 and a cache memory 22. The cache memory 22 may be temperature sensitive. As examples, the temperature sensitive cache memory may be a ferroelectric polymer memory or a flash memory.

The memory 22 may include a temperature sensor 24 in one embodiment of the present invention. The temperature sensor 24 may be a silicon diode formed on or integrated into the memory 22 in one embodiment.

Although a particular architecture is illustrated in Figure 1, the present invention is dependent on no particular architecture. Thus, a wide variety of other processor-based architectures may be utilized in other embodiments.

The processor 12 may include a storage 14 that stores a cache driver 14 that executes on the processor 12. The cache driver 14 adapts the processor-based system 10 to the vagaries of the cache memory 22 and, particularly, to its temperature sensitivity. For example, in one embodiment, when the temperature rises, and the memory 22 has a slower data transfer rate, the cache driver 14 may enable the system to adapt. The driver 14 itself may adapt to make more optimal decisions about what data to cache and not cache based on its knowledge of the cache's current data rate in view of the detected temperature.

Whenever the driver 14 makes a request to the cache memory 22, a status code is returned. This status code includes whether the operation succeeded or failed, whether error correction was applied, how much was applied, and the cache's temperature environment.

Referring to Figure 2, normal operation is indicated at the state 26. In normal operation, the memory 22 may be

a write-back cache. In a write-back cache, modifications to data in the cache are not copied to the disk drive 20 or other cache source and the cache simultaneously. In a write-through cache those changes may start to be written simultaneously, but since the disk drive is much slower, the operation takes longer, and thus the performance is lower.

The system 10 transitions from the normal operation state 26, to a reduced speed operation state 28, for example when the cache memory 22 is exposed to an elevated temperature environment called the throttle temperature range. In one embodiment, the temperature sensor 24 may detect that a higher temperature environment has been encountered. This higher or throttle temperature environment may be a temperature in the range of 60 to 80°C in an embodiment where the cache memory 22 is a ferroelectric polymer memory.

In this throttle temperature range, the cache memory 22 may be exposed to voltage disturbs if it does not reduce its data transfer rate. A voltage disturb is a voltage that causes data to be written incorrectly. The use of the memory 22 may be adjusted for reduced speed operation, if any, at state 28. For example, in one embodiment, the cache driver 14 may avoid operations like pre-fetching or other speculative data acquisitions that may necessitate higher data transfer rates than the cache memory 22 can

currently support. Also, the timing of the control logic on the memory 22 may be slowed down.

From the reduced speed operation state 28, the system may transition to an operation safe for sudden shutdown state 30. This may occur when the temperature becomes even more elevated. In one embodiment, using a cache memory 22 that is a ferroelectric polymer memory, the state 30 may be encountered at a critical temperature of 80 to 85°C.

In the state 30, the system 10 switches to a write-through caching algorithm and dirty cache lines (i.e., those that have not been written to system memory) are flushed. The system 10 may be close to the upper temperature or shutoff temperature of the cache memory 22. Thus, the cache driver 14 software or its hardware equivalent, changes algorithms so that it can shut off at any time without compromising data integrity. The driver 14 may cause the memory 22 to operate as a write-through cache rather than a write-back cache so that there is no dirty data in the cache.

The next transition, to the cache shutdown state 32, may occur at a shut-off temperature of about 85°C in the embodiment in which the cache memory 22 is a ferroelectric polymer memory. In this transition, cache lines may be invalidated and the cache memory 22 may be shut off.

The system 10 then waits for a reduced or critical temperature range to introduce hysteresis in state 34. Alternatively, the system may wait until a reboot/resume

before resuming reduced speed cache operations. From the hysteresis state 34, the system 10 may transition back to reduced speed operation state 28 by initializing a cache state, beginning the use of the cache, and using reduced speed algorithms. In the reduced speed operation state 28, with reduced temperature, the system 10 may adjust the algorithm for full speed operations, eventually returning, as indicated at F, to the normal operation state 26 at the normal temperature range.

Transitions may be spurred by the temperature sensor 24 that provides the temperature information to the cache driver 14 to appropriately control the operation of the system 10. For example, in the transition A, the temperature sensor 24 may indicate a throttle temperature range through the cache driver 14. The transition B may be initiated in response to a critical temperature range and the transition C may be indicated in response to the detection of a shutoff temperature. The transition D may be the result of a status indication of a critical temperature. The transition E may be the result of a status indication of a throttle temperature range, while the transition F may result from a status indication of a normal temperature range.

When the temperature sensed by the temperature sensor 24 is rising, the cache memory 22 is switched to write-through caching, so if the temperature rises further, and cache memory 22 shutdown is necessary, it can be done

without loss of data integrity. The cache memory 22 operates in a shutdown safe mode without dirty data in the cache. The critical range is set sufficiently below the shutdown temperature to allow margin for writing the dirty data before the temperature rises to shutdown.

If the temperature reaches the shutdown temperature, the cache memory 22 is no longer used. The contents of the cache memory 22 are invalidated so that, in case of a crash and recovery, it is clear that the contents of a cache memory 22 are invalid. As the temperature cools, there are two choices in some embodiments. Under one choice, the system 10 can wait until a reboot or resume to start up the cache memory 22 again. Alternatively, the system 10 can wait until the temperature is below the critical temperature. In either case, the cache memory 22 may be reinitialized and started from empty.

Referring to Figure 3, the cache driver 14, in one embodiment, may initially check to determine whether the throttle temperature was exceeded as indicated in diamond 36. If so, the operation of either the cache memory 22, the cache driver 14, or other components of the system 10 may be modified to adapt to the slower speed operation of the cache memory 22 as indicated in block 38.

Next, a check at diamond 40 determines whether or not a critical temperature has been exceeded. If so, the cache memory 22 may be switched to operate as a write-through

cache as indicated in block 42. Also, any dirty lines may be flushed as indicated in block 44.

Thereafter, the driver 14 monitors for the occurrence of a shutoff temperature as determined in diamond 46. If it is detected, the cache memory 22 may be shutdown as indicated in block 48. Thereafter, the memory 22 may transition back through a hysteresis state 34 to a reduced speed operation state 28, back to normal operation as shown in Figure 2.

Thus, despite temperature sensitivity, some memories can be used as cache memories, for disk caching purposes for example, when the operating range is less than the possible temperatures experienced in real life usage. In one such case, the cache memory 22 may be utilized as a disk cache to cache information read off the disk drive 20.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: